UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/650,195	08/29/2000	Feng-Jong Edward Yang	F0255	8593

45114 7590 09/03/2004

HARRITY & SNYDER, LLP
11240 WAPLES MILL ROAD
SUITE 300
FAIRFAX, VA 22030

EXAMINER	
BATES, KEVIN T	
ART UNIT	**PAPER NUMBER**
2155	

DATE MAILED: 09/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/650,195	YANG ET AL.	
	Examiner	Art Unit	
	Kevin Bates	2155	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,9-13 and 15-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 9-13, and 15-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to an Amendment filed on June 4, 2004.

Claims 1-7, 9-13, and 15-19 are pending in this office action.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 9, 10, 11, 13, 16, 17, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hassell (6208650) in view of Springer (4247920).

Regarding claim 1, Hassell discloses a network switch configured to control communication of data frames between stations (Column 5, lines 44 – 46), comprising: a plurality of receive devices corresponding to ports on the network switch (Column 6, lines 28 – 29), the receive devices configured to receive data frames from the stations (Column 6, lines 29 – 30); and an external memory interface configured to receive data from the plurality of receive devices (Column 6, lines 37 – 47); but Hassell does not explicitly indicate that the switch transfers a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the receive devices to a second memory, the external memory interface including a first external memory bus to transfer data to the first memory and a second external memory bus to transfer data to the second memory, the external memory interface being further configured to generate odd address information when

transferring data via the first external memory bus and even address information when transferring data via the second external memory bus. Springer teaches an external memory and an external memory interface that includes two memory devices, an even and an odd (Column 1, lines 63 – 67). If Springer's teachings were used to replace the external memory in Hassell, the combination would result in the switch transferring a portion of the data received from a first one of the receive devices to a first memory, and transfer a portion of the data received from a second one of the receive devices to a second memory (Springer, Column 2, lines 1 – 11) and the external memory interface including a first external memory bus to transfer data to the first memory and a second external memory bus to transfer data to the second memory (Figure 1, elements 58 and 54), the external memory interface being further configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus (Column 5, line 34 – Column 6, line 6, Springer generates the least significant bit of the address during the output process, which makes the address even or odd based on which memory module the output is coming from). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Springer's teachings in Hassell's switch in order to have memory modules that are accessible in parallel (Column 1, lines 63 – 65) without having a more complex addressing system (Column 2, lines 28 – 33).

Regarding claim 9, Hassell in combination with Springer discloses that the external memory interface is further configured to simultaneously retrieve data from the first and second memories (Springer, Column 2, lines 18 – 27).

Regarding claim 10, Hassell in combination with Springer discloses in a network: switch that controls communication of data frames between stations, a method of storing data frame information (Hassell, Column 5, lines 44 – 46), comprising: receiving a plurality of data frames; temporarily storing the received data frames in a plurality of receive devices (Hassell, Column 6, lines 28 – 29); and simultaneously transferring data frame information to at least a first memory and a second memory, wherein the simultaneously transferring includes: alternately transferring data frame information from a first group of the receive devices to the first and second memories, and alternately transferring data frame information from a second group of the receive devices to the first and second memories (Springer, Column 2, lines 1 – 11).

Regarding claim 11, Hassell in combination with Springer discloses simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices (Springer, Column 2, lines 18 – 27).

Regarding claim 13, Hassell in combination with Springer discloses that simultaneously transferring further includes: sending a portion of a first data frame via a first external memory bus and sending a portion of a second data frame via a second external memory bus (Figure 1, elements 58 and 54).

Regarding claim 15, Hassell in combination with Springer discloses that simultaneously retrieving data frame information from the first and second memories (Springer, Column 2, lines 18 – 27).

Regarding claim 16, Hassell in combination with Springer discloses a data communication system for controlling the communication of data frames between stations (Hassell, Column 5, lines 44 – 46), comprising: a plurality of receive devices configured to receive data frames from the stations (Hassell, Column 6, lines 28 – 29); a scheduler coupled to the plurality of receive devices and configured to generate selection signals to selectively output data frame information from the receive devices (Hassell, Column 6, lines 37 – 52); and a switching device configured to receive the data frame information and to simultaneously transfer data frame information from a first one of the data frames via a first external memory bus and data frame information from a second one of the data frames via a second external memory bus (Springer, Column 2, lines 1 – 11); a first memory configured to receive data frame information from the first external memory bus; and a second memory configured to receive data frame information from the second external memory bus (Springer, Figure 1, elements 58 and 54), wherein the switching device is further configured to: generate data address information having odd addresses for data transferred to the first memory and generate data address information having even addresses for data transferred to the second memory (Springer, Column 5, line 34 – Column 6, line 6).

Regarding claim 17, the combination of Hassel and Springer discloses that there are first and second multiplexers coupled to first and second groups of the receive devices, respectively, each of the first and second multiplexers being configured to receive the selection signals from the scheduler and to output a portion of a data frame (Figure 1, element 28, 32, and 38).

Regarding claim 18, the combination of Hassel and Springer discloses that the switching device is further configured to alternately transfer data received from the first multiplexer to the first and second external memory buses and to alternately transfer data received from the second multiplexer to the first and second external memory buses (Springer, Column 2, lines 1 – 11).

Regarding claim 19, the combination of Hassel and Springer discloses that the first memory is configured to store data words having odd addresses; and the second memory is configured to store data words having even addresses (Springer, Column 5, line 34 – Column 6, line 6).

Claims 2, 3, 4, 5, 6, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hassell in view of Springer as applied to claims 1, 9, 10, 11, 13, 16, 17, 18, and 19 above, and further in view of Gayton (5680401).

Regarding claims 2 and 4, Hassell in combination with Springer discloses that the external memory interface includes: a scheduler coupled to the receive devices and configured to enable the received data frames to be output to the first and second memories (Hassel, Column 6, lines 37 – 52), but does not explicitly indicate that the scheduler simultaneously outputting first and second selection signals for outputting data from the first receive device and the second receive device, respectively. Gayton teaches a scheduler, external memory interface, and external memory (Column 2, lines 50 – 52; Column 4, lines 57 – 59; Column 3, lines 52 – 54 where the arbiter is the scheduler). The scheduler allows the two memories to operate and deal with two different receive devices separately and simultaneously (Column 5, lines 16 – 18). It

would have been obvious to one of ordinary skill in the art at the time the invention was made to use Gayton's teaching of a plurality of external memories operating simultaneously in Hassell's switch in order to overlap operations thus increasing throughput (Column 2, lines 9 – 12).

Regarding claim 3, Hassell in combination with Springer discloses that the external memory interface is further configured to simultaneously transfer 8 bytes of data from the first receive device to the first memory and 8 bytes of data from the second receive device to the second memory (Column 7, lines 44 – 47).

Regarding claim 12, see the rejection to claims 2 and 3.

Regarding claim 4, Hassell in combination with Springer and Gayton discloses that the external memory interface is further configured to simultaneously transfer the portions of the data from the first and second receive devices to the first and second memories (Column 5, lines 16 – 18).

Regarding claim 5, Hassell in combination with Springer and Gayton discloses that the external memory interface is configured to simultaneously transfer data received from a first one of a first group of the receive devices via the first external memory bus and a second one of a second group of the receive devices via the second external memory bus (Column 5, lines 16 – 18).

Regarding claim 6, Hassell in combination with Springer discloses that the external memory interface is further configured to alternately transfer data received from the first group of receive devices to the first and second memories and to alternately

transfer data received from the second group of receive devices to the first and second memories (Springer, Column 2, lines 1 – 11).

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hassell in view of Springer in further view of Gayton as applied to claims 2, 3, 4, 5, 6, and 12 above, and further in view of Runaldue (6052751) (Applicants IDS).

Regarding claim 7, the combination of Hassell, Springer, and Gayton discloses that the first and second external memory buses are each 8-bytes wide (Springer, Column 7, lines 44 – 47), but does not explicitly indicate that the frequency is 100 MHz. Runaldo discloses that external memory can operate at 100 MHz (Column 5, line 32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Runaldo's teaching that external memory can operate at 100 MHz and enable Hassell's switch to interface with memory at that speed.

Response to Arguments

Applicant's arguments filed June 4, 2004 have been fully considered but they are not persuasive. The Applicant argues that the reference, Springer, does not teach generating odd and even address information for accessing a first and second memory and also does not teach alternately transferring data frames from a first received device to the first and second memories and alternately transferring data frames from a second received device to the first and second memories.

The examiner disagrees, the reference Springer discloses the ability to write 8 bit data addressed to an odd memory space into an odd memory, to write 8 bit data addressed to even memory into an even memory, and to write a 16 bit word into 8 bit

additions to the even and odd memories (Column 5, lines 37 – 53; Figures 1 and 2). Because of this operation, when the scheduler stores odd addressed data, that data gets sent across the memory bus that corresponds to odd memory, and the same with even addressed memory, this is the same as generating odd address information when transferring via the first memory bus as seen in the specification on page 7, line 24 to page 8, line 7.

As for the idea that Springer does not teach alternately transferring data frames from a first received device to the first and second memories and alternately transferring data frames from a second received device to the first and second memories. The examiner believes that the applicant is arguing the art individually and not as a combination. The combination of Hassell and Springer in the rejection to claim 10, discloses Hassell's switch that has a plurality of received devices that each access an external memory to store data frames (Column 6, lines 28 – 29; Column 6, lines 37 – 47) and if Springer's teaching of accessing external memory from an interface teaches that the external interface information to either even or odd memory or both memories at once (Column 2, lines 1 – 17). Through the combination of those two, when Hassell devices to store a data frame from the first memory onto the external memory it can be sent to both external memories simultaneously, and the same for the second receive device, thus giving the functionality of alternatively sending data from both receiving devices to both memories at once.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Bates whose telephone number is (703) 605-0633. The examiner can normally be reached on 8 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hosain Alam can be reached on (703) 308-6662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KB

KB
September 1, 2004

HOSAIN ALAM
SUPERVISORY PATENT EXAMINER